WHAT IS CLAIMED IS:

1. A power-on reset circuit comprising:

a power supply voltage detection circuit that detects a rise of a power supply voltage to a predetermined voltage and that causes a logic level of a first internal node from a first level to a second level;

a capacitor charge/discharge circuit that discharges a capacitor when the logic level of the first internal node of the power supply voltage detection circuit is the first level and that charges the capacitor via a resistor when the logic level is the second level; and

a reset pulse generation circuit that before the power supply voltage rises higher than the predetermined voltage, outputs a first output voltage to an output node and that after the power supply voltage has risen higher than the predetermined voltage, outputs a second output voltage to the output node upon detecting that a charge level of the capacitor has become higher than a charge level detection voltage,

wherein in an event that the power supply voltage is reduced, the capacitor charge/discharge circuit discharges the capacitor to follow the event, regardless of the logic level of the first internal node.

2. The power-on reset circuit as claimed in claim 1, wherein the reset pulse generation circuit outputs the second output voltage to the output node and reduces a set value of the charge level detection voltage.

3. The power-on reset circuit as claimed in claim 1, further comprises a power reduction circuit that after the reset pulse generation circuit has output the second output voltage, blocks a DC (direct current) current path occurring in the power supply voltage detection circuit.

4. The power-on reset circuit as claimed in claim 1, wherein

the power supply voltage detection circuit comprises:

a first diode circuit provided between a power supply line for supplying the power supply voltage and a second internal node to serve in a forward direction from the power supply line to the second internal node;

a first pulldown circuit provided between the second internal node and a ground line for supplying a ground potential;

a first pullup circuit provided between the first internal node and the power supply line to impart the first level to the logic level of the first internal node; and

a second pulldown circuit that is provided between the first internal node and the ground line and that is controlled by a voltage level of the second internal node for current driving capability,

wherein when the power supply voltage has risen higher than the predetermined voltage, the voltage of the second internal node becomes higher than a threshold voltage that is lower than the predetermined voltage and that is determined by circuit characteristics of the first diode circuit and the first pulldown circuit, whereby the current driving capability of the second pulldown circuit is increased to change a logic level of the internal output node to the second level.

5. The power-on reset circuit as claimed in claim 4, further comprises a power reduction circuit that after the reset pulse generation circuit has output the second output voltage, blocks current paths of the first pulldown circuit and the first pullup circuit of the power supply voltage detection circuit.

6. The power-on reset circuit as claimed in claim 1, wherein the capacitor charge/discharge circuit is composed in the manner that:

a second pullup circuit to be controlled by the voltage level of the first internal node for current driving capability, the resistor, and a third pulldown circuit to be controlled by the voltage level of the first internal node are series connected between the power supply line for supplying power supply voltage and the ground line for supplying the ground voltage;

the capacitor is connected between a third internal node, which is a connection junction of the resistor and the third pulldown circuit, and the ground line; and

a third diode circuit forming the discharge circuit serving in a forward direction from the third internal node to the power supply line is connected between the power supply line and the third internal node.

7. The power-on reset circuit as claimed in claim 1, wherein the reset pulse generation circuit comprises:

an inverter circuit in an initial stage for inputting the charge level of the capacitor as an input voltage and outputting a negation logic level thereof; and

a transistor for imparting hysteresis characteristics to the inverter circuit.

8. The power-on reset circuit as claimed in claim 1, wherein:

the capacitor charge/discharge circuit is composed so that at least one of a capacitance value of the capacitor and a resistance value of the resistor can be changed; and

the reset pulse generation circuit outputs the first output voltage of a

pulse width larger than a length that is determined by the charge level detection voltage, the capacitance value of the capacitor, and the resistance value of the resistor.